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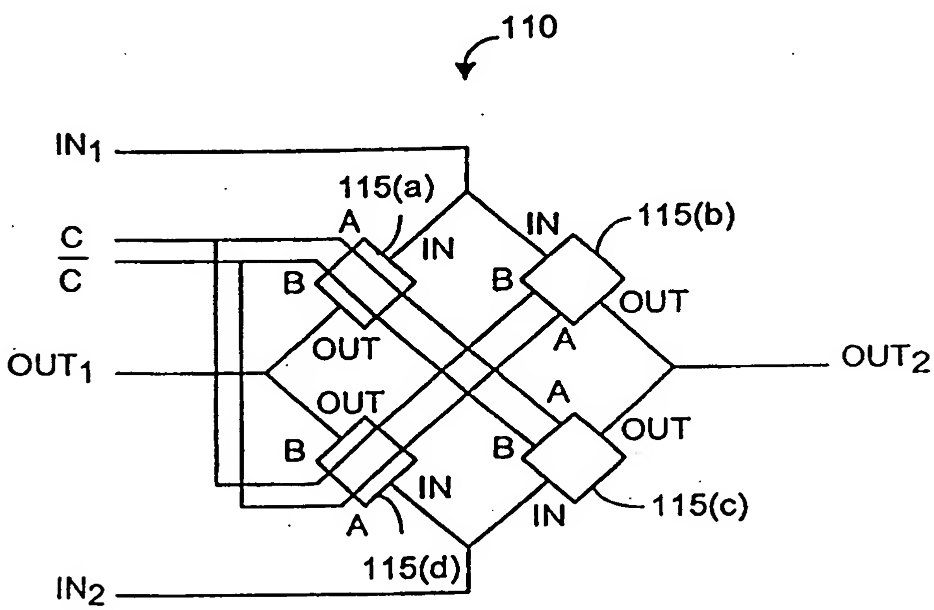

(57) Abstract

A switching network for routing multiple high-frequency digital signals that includes a plurality of interconnected T-switches. In one embodiment of the present invention, the switching network comprises one or more crossbar switches composed of these T-switches. The crossbar switches may be configured to provide any desired switching topology.

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HIGH-SPEED SWITCHING NETWORK USING T-SWITCHES

Brief Description of the Invention

The present invention relates generally to switching networks. More particularly, the present invention relates to a switching network for routing high-frequency digital signals using T-switches that are intended for switching RF or microwave signals.

Background of the Invention

As the clock speed of data communication signals continues to rise, it becomes increasingly difficult for switching networks to handle the routing of these signals. For example, the fiber optic-based SONET network standard produces very fast serial data streams with data transmission rates of up to 10 Gb/s. Switching networks are typically unable to transmit such high-frequency signals without first demultiplexing the signals because the commodity CMOS-based digital logic circuits used to implement the switches do not have sufficiently fast switching speeds.

In view of the shortcomings of prior art switching networks for routing high-frequency digital signals, it is an object of the present invention to provide a switching network that is capable of routing such signals and yet is relatively inexpensive to implement.

Summary of the Invention

The present invention is a switching network for routing multiple high-frequency digital signals that includes a plurality of interconnected T-switches. The T-switch is a switch that is widely used in wireless communication devices and instrumentation for switching high-frequency analog signals, such as RF and microwave signals. Each T-switch includes: (1) a first series transistor having a source for receiving a digital input signal, a gate for receiving a first control signal and a drain, (2) a second series transistor having a source coupled to the drain of the first series

transistor, a gate for receiving the first control signal and a drain for generating a digital output signal and (3) a shunt transistor having a drain coupled to the drain of the first series transistor and the source of the second transistor, a gate for receiving a second control signal and a source coupled to a ground voltage source.

In one embodiment of the present invention, the switching network comprises one or more crossbar switches composed of these T-switches. The crossbar switches may be configured to synthesize any desired switching topology for the switching network.

By using T-switches to construct the switching network, the present invention is capable of routing high-frequency digital signals and yet is relatively inexpensive to implement.

Brief Description of the Drawings

For a better understanding of the nature and objects of the invention, reference should be made to the following detailed description taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram of a crossbar switch in accordance with an embodiment of the present invention including four T-switches.

FIG. 2 is a circuit diagram of the T-switch used in the crossbar switch of FIG. 1.

FIG. 3 is a block diagram of a switching network using the crossbar switch of FIG. 1.

Like reference numerals refer to corresponding parts throughout the several views of the drawings.

Detailed Description of the Invention

FIG. 1 shows a 2 x 2 crossbar switch 110 in accordance with an embodiment of the present invention. The crossbar switch 110 is a double-pole, double-throw (DPDT) switch, a configuration that is well-known in the art. The crossbar switch selectively routes a first digital input signal received by the input IN_1 and a second digital input signal received by the input IN_2 between the two outputs OUT_1 and OUT_2. The routing of the first and second digital input signals is controlled by a first control signal

received by a first control input C and a second control signal received by a second control input $\overline{C}$, as described further below. Other embodiments of the crossbar switch 110 may have a different number of inputs, outputs or control signals.

The crossbar switch 110 is implemented with a plurality of T-switches 115. The T-switch 115 is a switch that is widely used in wireless communication devices and instrumentation for switching high-frequency analog signals, such as RF and microwave signals, and is of relatively low-cost. In the crossbar switch 110, however, the T-switch 115 is used for switching digital signals (i.e., signals having two voltage levels representing a logic "0" and a logic "1"). By using T-switches as the switching elements, the crossbar switch 110 is capable of transmitting very high frequency digital signals having clock speeds of up to about 12 GHz. The crossbar switch 110 may thus be used to construct a switching network capable of transmitting high-speed serial data streams (e.g., 2.5 to 10 Gb/s) such as those produced by networks using the SONET standard.

As shown in FIG. 2, each T-switch 115 includes an input IN, an output OUT, a first control input A and a second control input B. Referring again to FIG. 1, a first T-switch 115(a) is connected as follows: the input IN is connected to the input IN_1 of the crossbar switch 110, the output OUT is connected to the output OUT_1 of the crossbar switch, the first control input A is connected to the first control input C of the crossbar switch and the second control input B is connected to the second control input $\overline{C}$ of the crossbar switch. A second T-switch 115(b) is connected as follows: the input IN is connected to the input IN_1 of the crossbar switch 110, the output OUT is connected to the output OUT_2 of the crossbar switch, the first control input A is connected to the second control input $\overline{C}$ of the crossbar switch and the second control input B is connected to the first control input C of the crossbar switch. A third T-switch 115(c) is connected as follows: the input IN is connected to the input IN_2 of the crossbar switch 110, the output OUT is connected to the output OUT_2 of the crossbar switch, the first control input A is connected to the first control input C of the crossbar switch and the second control input B is connected to the second control input $\overline{C}$ of the crossbar switch. A fourth T-switch 115(d) is connected as follows: the input IN is connected to the input IN_2 of the crossbar switch 110, the output OUT is connected to the output OUT_1 of the crossbar switch, the first control input A is connected to the second

control input $\overline{C}$ of the crossbar switch and the second control input B is connected to the first control input C of the crossbar switch. In one embodiment of the present invention, the crossbar switch 110 is the GaAs MMIC FET Transfer Switch, model AD004T2-00, manufactured by Alpha Industries (Woburn, Mass.). In this embodiment, the crossbar switch is implemented as a single integrated circuit.

The operation of the crossbar switch 110 will now be described. As mentioned earlier, the crossbar switch 110 connects the inputs IN_1 and IN_2 to either of the outputs OUT_1 and OUT_2. If the control signals at the first and second control inputs C and $\overline{C}$ are set to a "high" and "low" voltage, respectively, the input IN_1 will be coupled to the output OUT_1 and the input IN_2 will be coupled to the output OUT_2. Conversely, if the control signals at the first and second control inputs C and $\overline{C}$ are set to a "low" and a "high" voltage, respectively, the input IN_1 will be coupled to the output OUT_2 and the input IN_2 will be coupled to the output OUT_1. The operation of the crossbar switch 110 is summarized by the truth table shown in Table 1. In the embodiment of the crossbar switch 110 mentioned above, the "high" voltage is 0 V and the "low" voltage is -7 V.

TABLE 1

C	$\overline{C}$	OUT_1	OUT_2
high	low	IN_1	IN_2
low	high	IN_2	IN_1

FIG. 2 is a circuit diagram of the T-switch 115 used in one embodiment of the crossbar switch 110. The T-switch 115 is a single-pole, single-throw (SPST) switch that is used to transmit RF or microwave signals and is commonly used in analog communication devices. The T-switch 115 includes an input IN, an output OUT, a first control input A and a second control input B. The T-switch comprises three MESFET transistors 121, 123 and 125 arranged in the so-called T-configuration commonly seen in RF and microwave attenuators. The first series transistor 121 is connected as follows: the source is connected to the input IN and the gate is connected to the first control input A through a first resistor 122. The second series transistor 123 is connected as follows: the source is connected to the drain of the first series transistor

121, the gate is connected to the first control input A through a second resistor 124 and the drain is connected to the output OUT. The shunt transistor 125 is connected as follows: the drain is connected to the drain of the first series transistor 121 and the source of the second series transistor 123, the gate is connected to the second control input B through a third resistor 126 and the source is coupled to a ground voltage source. The shunt transistor 123 is used to discharge accumulated charges at the node between the two series transistors 121 and 123.

Although the T-switch 115 is intended for switching RF or microwave analog signals, the switch has several properties that make it suitable for switching high-frequency digital signals. First, the bandwidth of the switch 115 typically ranges from DC to several Gigahertz. The wide frequency response of the switch enables the switch to transmit digital signals having clock speeds of up to several Gigahertz, such as those produced by networks using the SONET standard. The DC coupling of the switch allows the switch to transmit digital signals that may stay at one logic level for relatively long periods of time. Second, the off-state isolation of the switch 115 is typically in the range of 20 dB to 50 dB. The relatively high level of isolation provided by the switch enables multiple stages of switches to be connected in a switching network without introducing crosstalk between the paths in the network. Finally, the on-state resistance of the switch 115 is typically in the range of a few ohms. The relatively low resistance of the switch enables several stages of switches to be connected in a switching network without significant signal attenuation.

Continuing to refer to FIG. 2, the operation of the T-switch 115 to transmit a digital input signal is as follows. Since the operation of the switch for digital signals is similar in most respects to that for analog signals, it will be described only briefly. To place the switch 115 in the "on" state (i.e., the input IN is electrically coupled to the output OUT), the first and second control inputs A and B are set to the voltages 0 V and -7 V, respectively, to turn on series transistors 121 and 123 and turn off shunt transistor 125. To place the switch 115 in the "off" state (i.e., the input IN is electrically decoupled from the output OUT), the first and second control inputs A and B are set to the voltages -7 V and 0 V, respectively, to turn off series transistors 121 and 123 and turn on shunt transistor 125.

The switch 115 receives a digital input signal at the input IN having a logic "high" voltage of -0.9 V and a logic "low" voltage of -1.8 V. More generally, to ensure that the switch 115 transmits the digital input signal properly, the digital input signal should have a logic "high" voltage that does not exceed the control signal voltage used to turn on the transistors 121, 123 and 125 (e.g., 0 V) and a logic "low" voltage that is about 5 V or more greater than the control signal voltage used to turn off the transistors (e.g., -7 V). A standard logic signal with CMOS, PECL, HSTL or other standard logic levels generated by an external circuit (not shown) may be input to the switch 115 by first converting the logic levels of the signal using an input amplifier and level shifter 135 (see FIG. 3) to the voltage levels just specified. The digital output signal generated at the output OUT has approximately the same logic levels as the digital input signal received at the input IN. The digital output signal may be converted to standard logic levels for processing by an external circuit (not shown) using a limiting amplifier and level shifter 139 (see FIG. 3).

FIG. 3 shows a switching network 130 including a plurality of input amplifiers/level shifters 135, a switching fabric 137 and a plurality of limiting amplifiers/level shifters 139. The switching network 130 may be, for example, a routing switch in a high-speed data network. The switching network 130 selectively routes a plurality of standard logic input signals having standard logic levels from the inputs IN_1', IN_2', . . . , IN_n' to the outputs OUT_1', OUT_2', . . . , OUT_n'. The switching fabric 137 is composed of a plurality of crossbar switches 110. The crossbar switches 110 may be used to synthesize any desired switching topology for the switching fabric 137, as is known in the art. If the switching fabric 137 contains multiple stages of crossbar switches 110, amplifiers (not shown) may be placed between the stages to restore the amplitude of the digital signals as they are transmitted through the switching fabric.

The input amplifiers/level shifters 135 and the limiting amplifiers/level shifters 139 provide an interface between the switching fabric 137 and standard logic circuits external to the switching network 130 (not shown), as mentioned earlier. The input amplifiers/level shifters 135 each convert a standard logic input signal having standard logic levels to a digital input signal with voltage levels compatible with the T-switches 115 of the switching fabric 137. Conversely, the limiting amplifiers/level shifters 139

each convert a digital output signal output by the switching fabric 137 to a standard logic output signal having standard logic levels.

The foregoing description, for purposes of explanation, used specific nomenclature to provide a thorough understanding of the invention. However, it will be apparent to one skilled in the art that the specific details are not required in order to practice the invention. Thus, the foregoing descriptions of specific embodiments of the invention are presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed; obviously many modifications and variations are possible in view of the above teachings. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the following Claims and their equivalents.

IN THE CLAIMS:

1. A switching network for routing a plurality of high-frequency digital signals, comprising:

a plurality of interconnected T-switches configured in a switching network for high-frequency digital signals, each T-switch including:

a first series transistor having a source for receiving a digital input signal, a gate for receiving a first control signal and a drain;

a second series transistor having a source coupled to said drain of said first series transistor, a gate for receiving said first control signal and a drain for generating a digital output signal; and

a shunt transistor having a drain coupled to said drain of said first series transistor and said source of said second series transistor, a gate for receiving a second control signal and a source coupled to a ground voltage source.

2. The switching network of claim 1, wherein said first and second series transistors and said shunt transistor are field-effect transistors composed of gallium arsenide.

3. The switching network of claim 1, further comprising:

a plurality of input interface circuits coupled between a first external circuit and said plurality of interconnected T-switches, each input interface circuit converting a standard logic input signal received from said first external circuit to a digital input signal with voltage levels compatible with said T-switches; and

a plurality of output interface circuits coupled between said plurality of interconnected T-switches and a second external circuit, each output interface circuit converting a digital output signal received from said plurality of interconnected T-switches to a standard logic output signal with voltage levels compatible with said second external circuit.

4. A crossbar switch, comprising:

a first T-switch (115(a)) including an input for receiving a first digital input signal, an output for generating a first digital output signal, a first control input for receiving a first control signal and a second control input for receiving a second control signal;

a second T-switch (115(b)) including an input coupled to said input of said first T-switch, an output for generating a second digital output signal, a first control input for receiving said second control signal and a second control input for receiving said first control signal;

a third T-switch (115(c)) including an input for receiving a second digital input signal, an output coupled to said output of said second T-switch, a first control input for receiving said first control signal and a second control input for receiving said second control signal; and

a fourth T-switch (115(d)) including an input coupled to said input of said third T-switch, an output coupled to said output of said first T-switch, a first control input for receiving said second control signal and a second control input for receiving said first control signal.

5. The crossbar switch of claim 4, wherein said first, second, third and fourth T-switches each comprise:

a first series transistor having a source coupled to said input of the respective T-switch, a gate coupled to said first control input of the respective T-switch and a drain;

a second series transistor having a source coupled to said drain of said first series transistor, a gate coupled to said first control input of the respective T-switch and a drain coupled to said output of the respective T-switch; and

a shunt transistor having a drain coupled to said drain of said first series transistor and said source of said second series transistor, a gate coupled to said second control input of the respective T-switch and a source coupled to a ground voltage source.

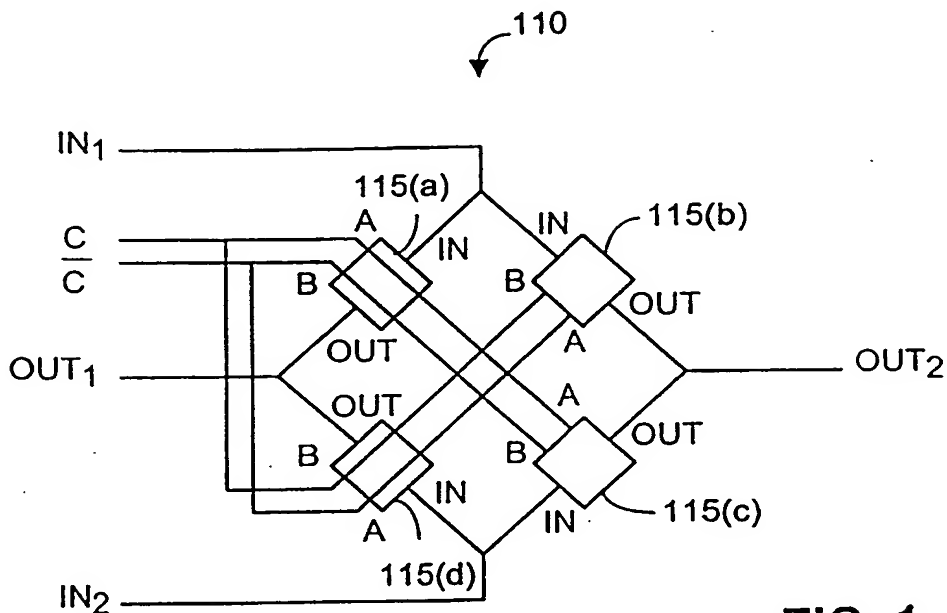
110
IN_1
115(a)
A
IN
115(b)
C
$\overline{C}$
B
B
OUT
A
OUT
OUT_1
OUT_2
A
OUT
OUT
B
B
IN
115(c)
A
IN
115(d)
IN_2

FIG. 1

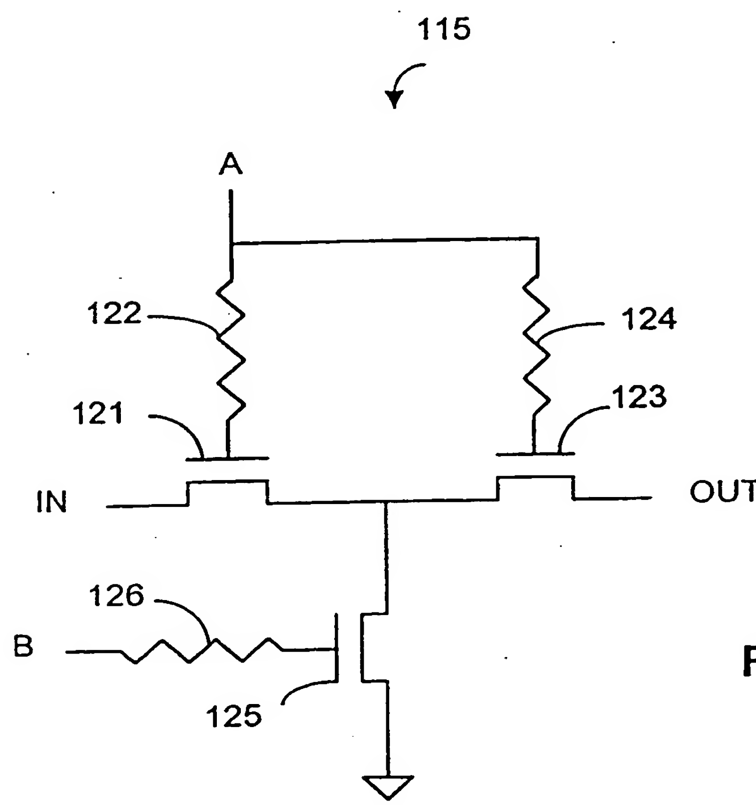
115
A
122
124
123
121
IN
OUT
126
B
125

FIG. 2

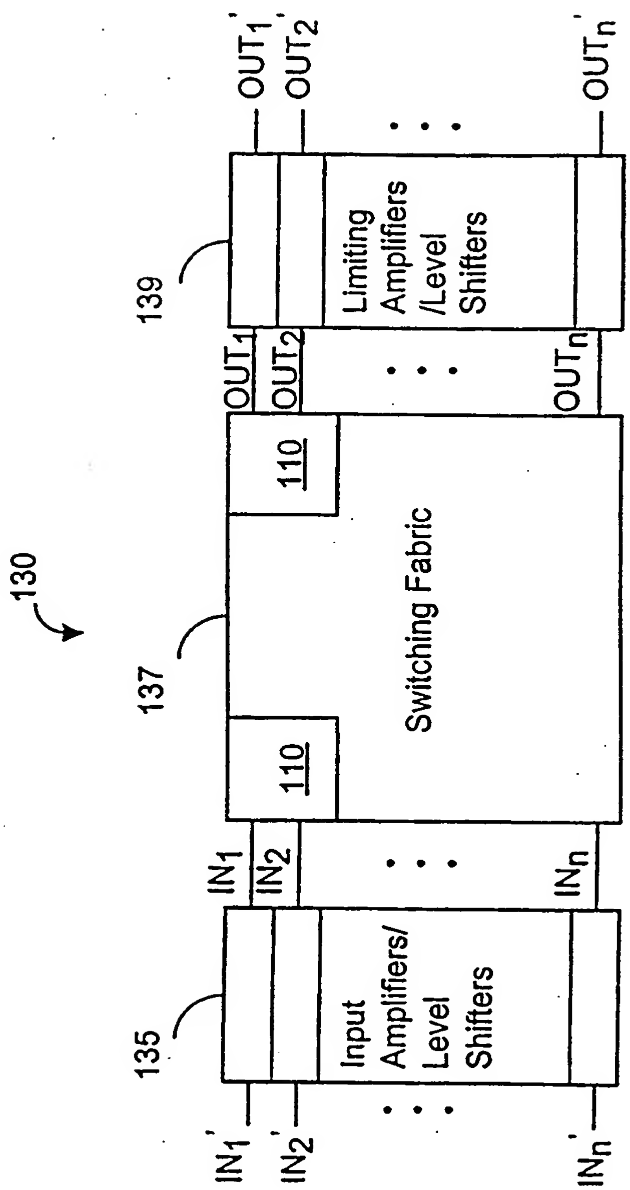
130
135
137
139
IN1'
IN2'
INn'
Input Amplifiers/ Level Shifters
IN1
IN2
INn
110
110
Switching Fabric
OUT1
OUT2
OUTn
Limiting Amplifiers /Level Shifters
OUT1'
OUT2'
OUTn'

FIG. 3

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/29726

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04Q3/52 H03K17/693

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04Q H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 696 470 A (ASSAL F T ET AL) 9 December 1997 (1997-12-09) column 1, line 7-14 column 1, line 62 -column 2, line 31 column 3, line 35-45 column 3, line 55 -column 4, line 18 column 4, line 26-39 figures 1,2,4,5	1-5
Y	SAVARA R ET AL: "A 2.5GB/S 16X16 BIT CROSSPOINT SWITCH WITH FAST PROGRAMMING" IEEE GALLIUM ARSENIDE INTEGRATED CIRCUITS (GAAS IC) SYMPOSIUM, vol. 17, 29 October 1995 (1995-10-29), pages 47-48, XP000630147 NEW-YORK, USA ISBN: 0-7803-2967-8 the whole document	1-5

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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7 April 2000	25/04/2000

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Inter.   nal Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 008, no. 161 (E-257), 26 July 1984 (1984-07-26) & JP 59 061315 A (FUJITSU KK), 7 April 1984 (1984-04-07) abstract	1,2
A	SOKOLOWSKA E ET AL: "INTEGRATED ANALOG SWITCH MATRIX WITH LARGE INPUT SIGNAL AND 46DB ISOLATION AT 1GHZ" PROCEEDINGSS OF THE INTERNATIONAL IFIP-IEEE CONFERENCE ON BROADBAND COMMUNICATIONS,1 April 1996 (1996-04-01), pages 418-429, XP000702598 CANADA ISBN: 0-412-75970-5 the whole document	1,4

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter nal Application No
PCT/US 99/29726

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